

Dhanekula Institute of Engineering & Technology
Department of Electronics and Communication Engineering



DIET/7.5.1/FT 12

UG TIMETABLE

Name of the Program: B. Tech in ECE

Class/Sem: II B. Tech SEM-I

Section-C

A.Y: 2020-21

W.E. F: 17/08/2020

DAY	1 9:00-10:00	2 10:00-11:00	3 11:00-12:00	LUNCH	4 02:00-03:00	5 03:00-04:00
MON	EDC	MEFA	RVSP		SS	OOPS-JAVA
TUE	SS	EDC	STLD		OOPS-JAVA	COI
WED	STLD	OOPS-JAVA	SS		RVSP	MEFA
THU	SS	STLD	EDC		MEFA	RVSP
FRI	COI	OOPS-JAVA	RVSP		EDC	SS
SAT	MEFA	RVSP	STLD		COI	EDC

Theory	Faculty Name	Total Hours
Electronic Devices and Circuits(EDC)	Mr.K.Siva Nagendra	05
Switching Theory and Logic Design(STLD)	Mrs.K.L.Sowjanya	04
Signals and Systems(S & S)	Mr.K.V.Seshagiri Rao	05
Random Variables and Stochastic Process(RVSP)	Mr.P.Krishna Reddy	05
Object Oriented Design & Programming Using Java (OOPS-JAVA)	Mrs.Ch.Padmini	04
Managerial Economics & Financial Analysis(MEFA)	Mrs.Ch.Gayatri	04
Constitution of India(COI)	Mrs.M.Silpa	03
Class In charge	Mr.K.V. Seshagiri Rao	

Pd
13/8/2020
I/C Timetables/Date



HOD
Date
HEAD OF THE DEPARTMENT
Electronics & Communication Engineering
DHANEKULA INSTITUTE
OF ENGINEERING AND TECHNOLOGY
Ganguru, VIJAYAWADA-521 139

Principal
Principal
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