

**Dhanekula Institute of Engineering & Technology**  
**Department of Electronics and Communication Engineering**



DIET/7.5.1/FT 12

**UG TIMETABLE**

Name of the Program: B. Tech in ECE

Class/Sem: II B. Tech SEM-I

Section-B

A.Y: 2020-21

W.E. F: 17/08/2020

DAY	1 9:00-10:00	2 10:00-11:00	3 11:00-12:00	LUNCH	4 02:00-03:00	5 03:00-04:00
MON	SS	COI	STLD		MEFA	RVSP
TUE	OOPS-JAVA	SS	COI		EDC	MEFA
WED	MEFA	RVSP	EDC		OOPS-JAVA	STLD
THU	RVSP	OOPS-JAVA	SS		STLD	EDC
FRI	EDC	STLD	RVSP		SS	OOPS-JAVA
SAT	MEFA	EDC	RVSP		SS	COI

Theory	Faculty Name	Total Hours
Electronic Devices and Circuits(EDC)	Mr.K.Siva Nagendra	05
Switching Theory and Logic Design(STLD)	Mrs.K.L.Sowjanya	04
Signals and Systems(S & S)	Mr.A.Sivannarayana	05
Random Variables and Stochastic Process(RVSP)	P.Krishna Reddy	05
Object Oriented Design & Programming Using Java (OOPS-JAVA)	Mr.R.Phani Kishore	04
Managerial Economics & Financial Analysis(MEFA)	Mr.Y.Priya Sagar	04
Constitution of India(COI)	Mrs.K.A.Sasikala	03
<b>Class In charge</b>		<b>Mr.K.Siva Nagendra</b>

*Pd*  
I/C Timetables/Date



HEAD OF THE DEPARTMENT  
 Electronics & Communication Engineering  
**DHANEKULA INSTITUTE**  
 OF ENGINEERING AND TECHNOLOGY  
 Ganguru, VIJAYAWADA-521 139

*K.S.N*  
HOD/Date

*Principals*  
**DHANEKULA INSTITUTE**  
 OF ENGINEERING AND TECHNOLOGY  
 Ganguru, Vijayawada-521 139