DHANEKULA INSTITUTE OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Faculty Publications for Academic year: 2016-2017

S.No	Faculty Name	Paper / Book title	Events / Journals / Publisher
1	Dr.G.L.Madhumati	FPGA based wireless electronic security system with sensor interface through GSM	Journal of Theoretical and Applied Information Technology, ISSN: 1992-8645, E-ISSN: 1817-3195, 31st July 2016. Vol.89. No.2,PP. 489-494
2	Dr.G.L.Madhumati	Design of Dynamically Reconfigurable Input/output Peripheral based Wireless System	Indian Journal of Science and Technology, Vol 9(30), DOI: 10.17485/IJST/2016/v9i30/98694, August 2016, ISSN (Print) : 0974- 6846 ,ISSN (Online) : 0974-5645,Vol 9 (30),August 2016,pp.1-9
3	Dr.G.L.Madhumati	Design of Substantial Delay Block using Voltage Scaled CMOS Inverter and Transmission Gate blend	2016 International Conference on Microelectronics, Computing and Communications (MicroCom), IEEE Conference Publications: 978- 1-4673-6621-2/16/$31.00 ©2016 IEEE, Pages: 1-6,DOI: 10.1109/MicroCom.2016.7522463
4	Mr. K.Satya Kiran	Power Efficient Modulo Convolution	International Conference on Inventive Competition Technologies (ICICT 2016), 26th- 27th August 2016, Coimbatore.
5	Mr. CH.Mohan Sai Kumar	Non-Linear Denoising of Images using Wavelet Transform	International Journal of Computer Applications (0975 – 8887), Volume 148 – No.10, August 2016
6	Mr.S.Chandra Sekhar	Systematic Error Correcting Codes Implementation for Matching of Data Encoded	International Journal of Professional Engineering Studies (IJPRES) Volume - 8, Issue-2, January 2017. www.ijpres.com
7	Mr.M. Tulasidas	New framework to enhance the quality of image using gradient domain guided image filtering	International conference on contemporary engineering and technology-2017.March 2017
8	Mr.M. Tulasidas	Multilevel local extrema method on medical image processing	International conference on contemporary engineering and technology-2017. March 2017.

9	Mr. V. Subba Raju	FPGA Implementation of 32-Bit Partially Parallel Encoder Architecture for Long Polar Codes	International Journal of Research(IJR), P-ISSN: 2348-6848 E-ISSN: 2348-795X Volume 03 Issue 18 December 2016.
10	Mrs.T.Haritha	Design And Implementation Of Flexible Computational Unit Using Carry Save Adder	International Journal of Professional Engineering Studies (IJPRES), Volume VII /Issue 5 / Nov 2016.
11	Mrs.M.Mythri	FFT Implementation of Multi-Precision Based Dynamic Voltage Scaling Multiplier with Operands Scheduler	International journal& magazine of engineering, technology, management and research (IJMETMR). ISSN:2348-4845,Volume.03,IssueNo.12, December-2016, Pages: 407-411
12	Dr.G.L.Madhumati	Area-Power Efficient Shift Register Using Non overlap Delayed Pulsed Clock	International Journal For Technological Research In Engineering(IJTRE), Volume 4, Issue 4, December-2016,ISSN (Online): 2347 - 4718
13	Mr.K.Suresh Babu	Design of low Power All Digital Phase Locked Loop for SerDes	International Journal of VLSI System Design and Communication Systems(IJVDCS) Volume.04, IssueNo.10, October- 2016, Pages: 0999-1003
14	Mrs.K.L.Sowjanya	Implementation of RISC Processor Using Radix-4 & Radix-8 Booth Encoded Multi-Modulus Multipliers	International journal& magazine of engineering, technology, management and research (IJMETMR). ISSN:2348-4845, Volume.03, Issue No.10, October-2016, Pages: 1631-1634
15	Mr.A.Sivannarayana	FIR Filter Implementation Using Novel Modulo 2n-2k-1 Adder for RNS	International journal& magazine of engineering, technology, management and research (IJMETMR). ISSN:2348-4845, Volume.03, Issue No.10, October-2016, Pages: 1626-1630
16	Dr.B.L.Prakash	Maximum Entropy method for estimation of tonal frequencies of seismic signals	National Conference on Knowledge based Inventive Tele communication Systems (NCKITS-2017),(16- 18) March 2017.