VLSI LABORATORY

Objective: The objective ofthis laboratory is to Design, implement and simulation of Combinational circuits, Sequential circuits, Analog circuits using CMOS 130nm Technology.

Sections Handled:

B.Tech IV Year I Semester – VLSI lab - ECE - A&B Sections

B.Tech II Year II Semester – Electronic Circuits lab - ECE - A&B Sections

Major Equipment Details:

S. No	Name of the Equipment/Make/Model No	Quantity
1.	DESKTOP PC Make: HP Model No: Pro 3090 Desk Top Computers Intel Core 2 Duo E7500@2.93GHz Processor, Intel G 43 MBD, 2 GB DDR III RAM, 320 GB HDD, 15.6" TFT LCD Monitor	20
2.	DESKTOP PC Make: HP Model No: HP Pro 3335 Desk Top Computers AMD Athlon II X2 255 Dual Core Processor @ 3.1GHz Processor, AMD 785G MBD, 4GB DDR III RAM, 500 GB HDD,18.5" HP LED Monitor	16
3.	Multisim V11.0 and Labview Software	15+1 Users
4.	Mentor Graphic's Higher Education Program1(HEP 1) IC Nanometer Design Tool setLicense for 3 Years	40 Users
5.	System Software : Windows -7 professional - Licensed	36
6.	Online UPS,10KVA Make: RESQ Make 1 X 10 KVA Online UPS with AMARON 20 12V – 26 AH Batteries with Minimum of 30 Min hours Back up	1
	Total Cost	**Rs. 14,75,000.00**

Faculty Incharge with qualification: Mr.K.Ramakoteswara Rao, M.Tech

Lab Technician name with qualification: Mrs.D.Ramya, B.Tech

Experiment list as per curriculum:

1. Design and Implementation of an Inverter.
2. Design and Implementation of Universal gates.
3. Design and Implementation of Full Adder.
4. Design and Implementation of Full Subtractor
5. Design and Implementation of RS-latch
6. Design and Implementation of D-latch.
7. Design and Implementation of Asynchronous counter.
8. Design and Implementation of Static RAM cell.
9. Design and Implementation of Differential Amplifier
10. Design and Implementation of Ring oscillator.
11. Design and Implementation of 2-input AND gate.
12. Design and Implementation of 2-input OR gate.

Experiment list beyond the curriculum

1. Design and Implementation of 2-input EX-OR gate.
2. Design and Implementation of 3-input NAND gate.
3. Design and Implementation of 3-input OR gate.
4. Design and Implementation of JK-Flip flop.