## VLSI DESIGN AND RESEARCH LABORATORY

**Objective:** The objective of this laboratory is to design and analyse digital circuits using CADENCE and other latest tools.

**Sections Handled:**

M.Tech I Year I Semester – Front End VLSI Design Lab - ECE

M.Tech I Year II Semester – Back End VLSI Design Lab - ECE

**Major Equipment Details:**

| S. No | Name of the Equipment/Make/Model No | Quantity |
|---|---|---|
| 1. | Desktop Computer<br>Make: HP Model No: HP Pro 3090 | 07 |
| 2. | Desktop Computer<br>Make: HP Model No: HP Pro 4000 SFF | 17 |
| 3. | Xilinx Software<br>Make: Xilinx Model No: v13.1 | 25 |
| 4. | Cadence Software<br>Make: Cadence Model No: UG3Y10L | 10 |
| 5. | UPS<br>Make: Eaton Model No: 9145, 6.0 KVA | 01 |
| 6. | UPS Batteries<br>Make: Amarraja Model No: 12V-42AH | 20 |
| 7. | RAM<br>Make: Hynix Model No: DDR3- 2GB RAM | 18 |
| 8. | XUP Vertex-5 with cable<br>Make: Core EL Technologies Model No: LX11OT with cable | 01 |
| 9. | Genesys V5- FPGA Kit<br>Make: Core EL Technologies Model No: V5 | 01 |
| 10. | CPLD<br>Make: Core EL Technologies<br>Model No: Cool Runner | 01 |
| 11. | VMOD- CAM, BB,WW, programming cable<br>Make: Core EL Technologies | 01 |
| | **Total Cost** | **Rs.13,79,650.43** |

**Faculty Lab In charge with qualification:** Mr.K.Suresh Babu, M.Tech

**Lab Technician name with qualification:** Mrs.D.Sirisha, B.Tech

**Experiment list as per curriculum:**

**Sem-I:**

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
9. Fire Detection and Control System using Combinational Logic circuits.
10. Traffic Light Controller using Sequential Logic circuits
11. Pattern Detection using Moore Machine.
12. Finite State Machine (FSM) based logic circuit

**Sem-II:**

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM

**Experiment list beyond the curriculum**