## DSD&DICA AND DSP LABORATORY

**Objective:** The objective of this laboratory is to design internal structure of the Digital Integrated Circuits, develop VHDL source code & verify functionality using simulation and to verify the designed Logic circuits using Spartan 6 FPGA Kits.



**Sections Handled:**

B.Tech III Year I Semester – DSD&DICA lab - ECE - A&B Sections

B.Tech III Year II Semester – DSP lab - ECE - A&B Sections

**Major Equipment Details:**

| S.No | Name of the Equipment/Make/Model No | Quantity |
|---|---|---|
| 1. | DESKTOP PCMake: HP<br>Model No: Pro 3090 Desktop Computer<br>Intel Core2 Duo E7500 @2.93 GHz Processor, Intel G43 MBD, 2GB DDR III RAM, 320 GB HDD,15.6" TFT LCD Monitor. | 36 |
| 2. | MATLAB SOFTWARE  R2011b | 10 |
| | Simulink Tool Box | 2 |
| | Signal Processing Tool Box | 2 |
| | Communication Tool Box | 2 |
| | DSP System Tool Box | 2 |
| 3. | TMS320C6713 DSP Starter Kit with CCSV3.1<br>Make: Spectrum DigitalModel No: 6713DSK Board | 6 |
| 4. | Xilinx System Edition 13.1Make : Xilinx | 25 |
| 5. | Altys Spartan-6 FPGA Kit<br>Make: DigilentModel:XC6SLX45 CSG324C | 4 |
| 6 | System software : Windows-7 Professional - Licensed | 36 |
| 7. | Online UPS,10KVA<br>Make: RESQ Make 1 X 10 KVA Online UPS with AMARON 20 12V -26AH Batteries with Minimum of 30 Min Hours Back up. | 1 |
| **Total Cost** | | **Rs.16,43,185.00** |

**Faculty Lab Incharge with qualification:** Mr.P.Krishna Reddy, M.Tech

**Lab Technician name with qualification:** Mr.B.Venkateswara Rao, B.Tech, M.Tech

**Experiment list as per curriculum:**

**Digital System Design & DICA Lab:**

1. Realization of Logic Gates.

2. Design and Verify 3 to 8 Decoder- 74138.

3.Design and Verify 8*1 Multiplexer-74151 and 2*1 De-multiplexer-74155

4.Design and Verify 4-Bit Comparator-7485.

5. Design and Verify D Flip-Flop- 7474.

6. Design and Verify Decade Counter- 7490.

7.Design and Verify 4 Bit Counter-7493.

8. Design and Verify Shift Register-7495.

9. Design and Verify Universal shift register-74194/195.

10.Design and Verify Ram (16*4)-74189 (read and write operations)

11. Design and Verify ALU.

**Digital Signal Processing Lab:**

1. To verify linear convolution.

2. To verify the circular convolution.

3. To design FIR filter (LP/HP) using windowing technique

4. Using rectangular window

5. Using triangular window

6. Using Kaiser Window

7. To design IIR Butterworth Digital (Low pass and High pass) Filter.

8. N-point FFT algorithm.

9. MATLAB program to generate sum of sinusoidal signals.

10. MATLAB program to find frequency response of analog LP/HP filters.

11. To compute power density spectrum of a sequence.

12. To find the FFT of given 1-D signal and plot.

13. To study the architecture of DSP chips – TMS 320C 5X/6X Instructions.

14.FIR Filters using TMS320C6713 DSK.

15. IIR Filters using TMS320C6713 DSK.

**Experiment list beyond the curriculum**

**Digital System Design & DICA Lab:**

1. Design of Fast Carry Look -Ahead Adder.

2. Design of a Boolean function using 8*1 Multiplexer

**Digital Signal Processing Lab:**

1. Generation of Basic Signals

2. IIR Butterworth Digital (Low pass and High pass) Filter - TMS 320C 5X/6X Instructions.

3. Linear Convolution using TMS320C6713 DSK.

4. Auto Correlation, Cross Correlation using Matlab.